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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,576	07/21/2003	Darel N. Emmot	10001771-3	7505

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EXAMINER	
MONESTIME, MACKLY	
ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,576	EMMOT ET AL.	
	Examiner	Art Unit	
	Mackly Monestime	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23* is/are allowed.

6)☒ Claim(s) *1-9 and 11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/21/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9, 11-14 and 15-23 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-9, 11-14, 15 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jinzaki (US Patent No. 4,975,833) in view of Wilkes (US Patent No. 5,448,698) and further in view of McKenney (US Patent No. 6,678,772).

4. Jinzaki and Wilkes were cited in IDS filed on July 21, 2003.

5. As per claims 1, 11 and 15, Jinzaki substantially disclosed the invention as claimed, including a system of integrated circuit defining a plurality of node and a memory connected to each node (Fig. 5; Group A and Group B), each node comprising: a t least one functional unit configured to carry out a predetermined processing function (Fig. 5; Group A and Group B), a communication mechanism configure to manage and control communication of information with other nodes (col. 3, lines 54-65); a memory controller configured to control writes to and reads from the memory connected to node (col. 2, lines 43-45).

Jinzaki did not explicitly disclose that the memory is a random access memory (RAM). However, Wilkes disclosed an inter-processor communication system having a

plurality of processing nodes wherein each processing node includes a processor and a local RAM connected therein (col. 4, lines 27-29). Moreover, RAM has the advantages that it typically resides on the same printed circuit board as the CPU/ processor, thus it provides the advantages of on-chip storage for storage intermediate results and eliminate time consuming external memory access operations and having a fast data access and also simultaneously perform reading and writing operations. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to have utilized a RAM into the system of Jinzaki because doing so would enhance the overall processing speed of the multi processing system.

The combination did not explicitly disclose wherein the system is further configured to permit read access to a memory by a plurality of processing nodes in the system, but is further configured to limit write access to a memory to only the node to which the memory is connected; but Jinzaki did teach the use a lock mechanism in the multiprocessing system, and when the lock is set only the active processor can write in its local memory (col. 2, lines 45-53). However, McKenney disclosed a multiprocessing system having a plurality of processors and executing multiple processes in parallel (col. 1, lines 14-16), and further disclosed a reader-writer lock which allows multiple reading processes ("readers") to access simultaneously a shared resource such as a database, while a writing process ("writer") must have exclusive access to the database before performing any updates for consistency (col. 2, lines 39-43). It would have obvious to one of ordinary skill in the art at the time the invention was made to combine

the cited references because doing so would prevent conditions that destroy the coherency of data, and thereby ensure data integrity within the multiprocessing system.

6. As per claim 4, Jinzaki disclosed that each node further includes control means for controlling the use and access of memory storage by remote functional unit (col. 3, lines 63-68; and col. 4, lines 1-3).

7. As per claims 5-6, 12 and 17-18, Jinzaki did not disclose that the control means includes a memory segment containing at least one work queue, the work queue being in the form of a first-in first-out instruction for the at least one functional unit; and the work queue contains a plurality of messages. However, Wilkes disclosed a memory having a plurality of records referred to as slots and a work queue wherein each slot stores information that describes the message area in the RAM (Fig. 2, Items No. 107-108); and the work queue contains a plurality of messages (col. 6, lines 50-53). It would have obvious to one of ordinary skill in the art at the time the invention was made to have included the work queue taught by Wilkes into the system of Jinzaki because doing so would provide a multi-processing computer system that is capable of working efficiently where there is a long latency from the time the data is requested and the time the data is available for use.

8. As per claims 7 and 13, Jinzaki disclosed wherein messages may be communicated between different nodes under control of the control means (col. 3, lines 54-68; col. 4, lines 1-3).

9. As per claims 8 and 14, Jinzaki disclosed that the plurality of nodes is interconnected via a plurality of serial communication link (Figs. 4-5, Items No. 6, 6', 7 and 7').

10. As per claim 9, Jinzaki did not disclose that the RAM is segmented to include at least one segment dedicated to the control means and one additional segment dedicated to carrying out a functional operation. However, Wilkes disclosed that the RAM is segmented to include at least one segment dedicated to the control means and one additional segment dedicated to carrying out a functional operation (col. 5, lines 41-49; col. 6, lines 10-16). It would have obvious to one of ordinary skill in the art at the time the invention was made to have implemented such features into the system of Jinzaki because doing so would provide a multi-processing computer system that is capable of working efficiently where there is a long latency from the time the data is requested and the time the data is available for use.

11. Claims 2-3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jinzaki in view of Wilkes and McKenney as applied to claim 1 above, and further in view of Horvitz et al (US Patent No. 6,232,974).

12. Horvitz et al were cited in IDS filed on July 21, 2003.

13. As per claims 2-3 and 16, the combination did not disclose that the system is a computer graphics system and wherein the at least one functional unit is one selected from the group consisting of a texture mapping, a geometry accelerator, a shader, a z-blend component, a rasterizer, a tiler and a cache controller. However, Horvitz et al disclosed that the system is a computer graphics system (col. 1, lines 8-10) and wherein

the at least one functional unit is one selected from the group consisting of a texture mapping, a geometry accelerator, a shader, a z-blend component, a rasterizer, a tiler and a cache controller (Figs. 13-14; col. 27, lines 41-46; col. 28, lines 11-53). It would have obvious to one of ordinary skill in the art at the time the invention was made to have utilized the processing unit or the functional unit or the processing node disclosed by Horvitz et al into the system of Jinzaki and Wilkes because doing would provide a more reliable multi- processing system being able to perform high performance graphics and geometry operations.

14. As per claim 19, Jinzaki substantially disclosed the invention as claimed, including a system of integrated circuit defining a plurality of node and a memory connected to each node (Fig. 5; Group A and Group B), each node comprising: a t least one functional unit configured to carry out a predetermined processing function (Fig. 5; Group A and Group B), a communication mechanism configure to manage and control communication of information with other nodes (col. 3, lines 54-65); a memory controller configured to control writes to and reads from the memory connected to node (col. 2, lines 43-45).

Jinzaki did not explicitly disclose that the memory is a random access memory (RAM); a memory segment containing at least one work queue, the work queue being in the form of a first-in first-out instruction for the at least one functional unit; and the work queue contains a plurality of messages. However, Wilkes disclosed an inter-processor communication system having a plurality of processing nodes wherein each processing node includes a processor and a local RAM connected therein (col. 4, lines 27-29), and

further disclosed a memory having a plurality of records referred to as slots and a work queue wherein each slot stores information that describes the message area in the RAM (Fig. 2, Items No. 107-108); and the work queue contains a plurality of messages (col. 6, lines 50-53). Moreover, RAM has the advantages that it typically resides on the same printed circuit board as the CPU/ processor, thus it provides the advantages of on-chip storage for storage intermediate results and eliminate time consuming external memory access operations and having a fast data access and also simultaneously perform reading and writing operations. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to have utilized a RAM into the system of Jinzaki because doing so would enhance the overall processing speed of the multi processing system.

The combination did not explicitly disclose wherein the system is further configured to permit read access to a memory by a plurality of processing nodes in the system, but is further configured to limit write access to a memory to only the node to which the memory is connected; but Jinzaki did teach the use a lock mechanism in the multiprocessing system, and when the lock is set only the active processor can write in its local memory (col. 2, lines 45-53). However, McKenney disclosed a multiprocessing system having a plurality of processors and executing multiple processes in parallel (col. 1, lines 14-16), and further disclosed a reader-writer lock which allows multiple reading processes ("readers") to access simultaneously a shared resource such as a database, while a writing process ("writer") must have exclusive access to the database before performing any updates for consistency (col. 2, lines 39-43). It would have

obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would prevent conditions that destroy the coherency of data, and thereby ensure data integrity within the multiprocessing system.

15. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kilgariff et al (US Patent No. 5,999,183) in view of Wilkes (US Patent No. 5,448,698).

16. As per claims 20-22, Kilgariff et al substantially disclosed the invention as claimed, including four nodes wherein each node comprises a memory couple to a functional unit and a processor, wherein the processor being coupled to the functional unit to direct data into in and out of the functional unit comprises a geometry accelerator coupled to a rasterizer and a memory controller (Fig. 5, Items No. 500_1-500_4; lines 12-32); and each of the four nodes being connected to the other three nodes through a communication link, and each of the four nodes adapted to send data from its memory to each of the other three nodes through the communication link (col. 5, lines 32-37).

Kilgariff et al did not explicitly disclose that the memory is a random access memory (RAM). However, Wilkes disclosed an inter-processor communication system having a plurality of processing nodes wherein each processing node includes a processor and a local RAM connected therein (col. 4, lines 27-29). Moreover, RAM has the advantages that it typically resides on the same printed circuit board as the CPU/ processor, thus it provides the advantages of on-chip storage for storage intermediate results and eliminate time consuming external memory access operations and having a fast data access and also simultaneously perform reading and writing operations. Therefore, it would have obvious to one of ordinary skill in the art at the time the

invention was made to have utilized a RAM into the system of Kilgariff et al because doing so would enhance the overall processing speed of the multi processing system.

Allowable Subject Matter

17. Claim 23 is allowable over the prior art of record.

The prior art of record failed to teach or suggest individually or in combination a method for performing geometry accelerator computations in a distributed, nodal architecture graphics systems, wherein the method comprises the uniquely distinct steps of: "distributing messages over a plurality of geometry accelerator work queues, propagating to an output of each geometry accelerator all messages that are directly executable by the geometry accelerators; and producing, by each geometry accelerator, a work queue for shaders, wherein the work queue for shaders comprise messages denoting drawing primitives" (as per claim 23). These distinct features of the present claims invention have not found to be anticipated, suggested or made obvious by the prior art of record, either singularly or in combination.

Conclusion

Applicant is required to give full consideration to these prior art references when responding to this office action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bridge et al (US Patent No. 6,125,368) taught fault tolerant timestamp generation for multi-node parallel database.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mackly Monestime whose telephone number is (703) 305-3855. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bella Matthew, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

or faxed to:

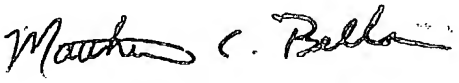
(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Mackly Monestime

Patent Examiner



MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

September 28, 2004